



# 100Gbps System Architecture

IO Utilization and Tradeoffs in an FPGA design example

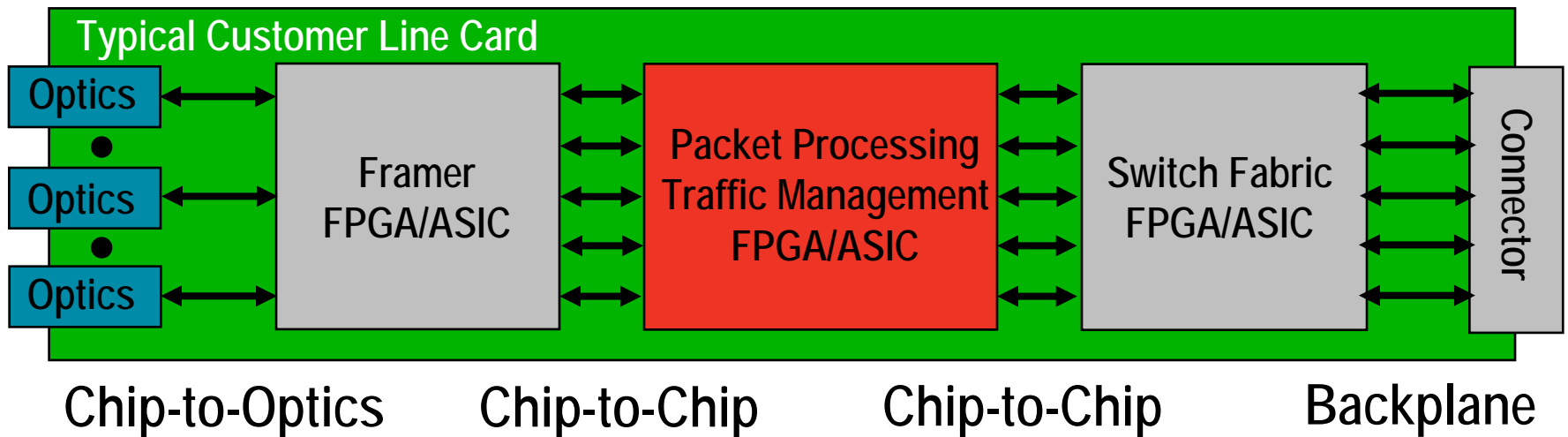
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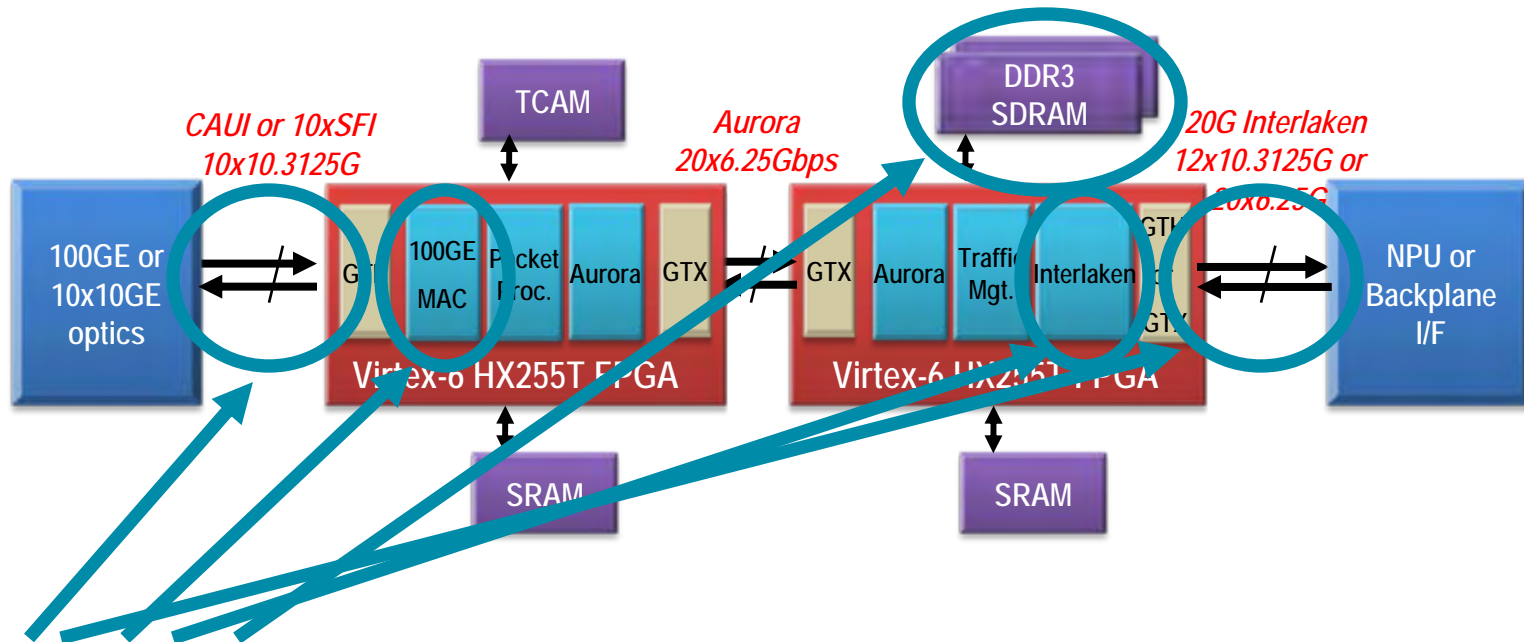
# Agenda

- **Line Card Architecture at 100Gbps**
- **Traffic Management Example at 100Gbps**
- **Implementation Challenges at 100Gbps**
- **Scaling Beyond 100Gbps**

# Line Card Architecture at 100Gbps



# 100Gbps Traffic Management Example

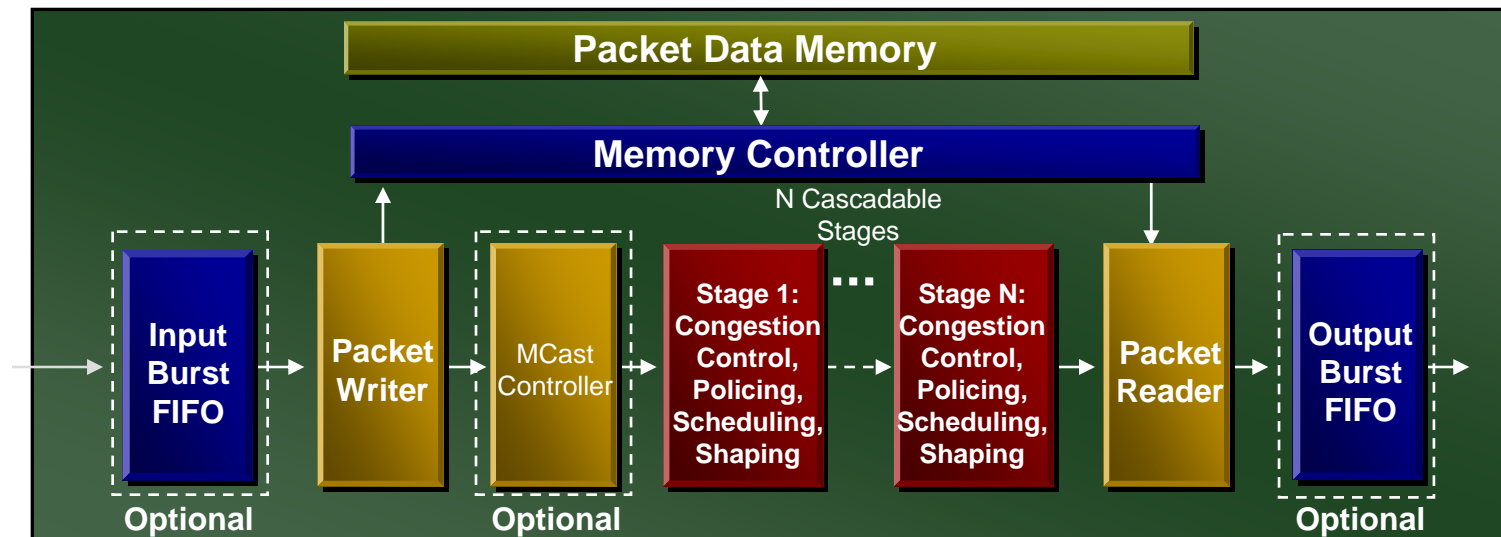


## 2. 100Gbps Signal Bandwidth

- 100GE MAC (10x10.3125Gbps) Virtex-6 HXT
- DDR3 SDRAM (Tr 24 limited 25Gbps)
- Requires ~540pins @ 1066Mbps DDR3 SDRAM

# 100Gbps Traffic Management Example

- **Traffic Manager IP core**
  - Released 2007
  - Many customers, in live networks today
- **Flexible And Scalable Traffic Manager IP Core**
  - Line Rate Up To 40 Gbps today, 100G in near future
- **Ideal For Metro, Access, And Enterprise Applications**
  - Targets Other Applications Such As Wireless Backhaul
- **Supports Both Virtex™ And Spartan™ Platforms**



# Implementation Challenges @ 100Gbps

## ▪ Packet Storage

- High Bandwidth => High Pin Count
- Cost
  - DDR3 SDRAM vs. RLDRAM2/3
- Random Access and Latency
  - TRC is an issue with bandwidth efficiency for DDR3 SDRAM
    - 66% bandwidth efficiency possible with optimized Xilinx memory controllers

## ▪ Descriptor Storage

- High queue counts force us out of FPGA block RAM
- Options to combine descriptor and packet storage

## ▪ Traffic Scheduling Speed

- Limited by # clock cycles needed to make a work-conserving decision
- FPGAs are typically limited by clock speed by non-parallelizable algorithms

## ▪ Power

- Customers doubling bandwidth without doubling slot power consumption
- Hardware implementations tend to be more power efficient vs. software
  - 50% lower than nearest NPU
- External memory IO power can be >50% of total power

# Scaling Beyond 100Gbps

## ▪ Key Challenges

- Need higher performance packet memory – pin limited at 200Gbps+
- Need faster state memory storage for larger queues
- Need ability to simulate SI issues more effectively

# Scaling Beyond 100Gbps

## ▪ **Faster Packet Memory : Serial Memories**

- Interlaken-LA “Interlaken Look-Aside”
  - Currently support interfaces to external “Network Search Engine” (TCAM)
  - Virtex-5 board with Netlogic NSE available today
- Other emerging standards
- Latency gets worse

## ▪ **Faster**

## ▪ **Advanced Simulation**

- Xilinx SERDES support IBIS-AMI models today
- Co-development with SiSoft for Virtex-5 models
- Virtex-6 models available later in 2010