Chip-Scale FBAR Oscillator for Data Communications

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Co-Integration, Co-Design of Timing Function

There has been strong, evolutionary pressure to integrate high quality clocking and frequency sources into the ASIC package.

FBAR Chip Scale Packaged (CSP) Oscillator:
- Very small size
- Low jitter
- High native frequency (500MHz to 5GHz)

The FBAR CSP oscillator is a high quality frequency and timing source. Because it is so small and thin, it can be integrated within a typical BGA ASIC package.
Leveraging FBAR Filter Technology

Low Jitter FBAR CSP Oscillator

Evaluating a Copper Link

Adding Optics for a Full System Test

Summary
Physics of Film Bulk Acoustic Resonators (FBAR)

Piezoelectric FBAR Resonator

Mo/AlN/Mo free-standing membrane

Au Pad

Si etch pit

Cross-Section

Electrical Analog

Sputter-deposited AlN

Top Electrode

Bottom Electrode

AIN

C_{MOTIONAL}

F_{MOTIONAL}

C_{SHUNT}

L_{MOTIONAL}
Band 7 LTE Co-Existence Duplexer (2.0 X 1.6 mm²)

- LTE Band-7 Duplexer
- Designed for ISM band (WiFi) coexistence
- Multiple Design Wins with our WiFi Coexistence Filter

63% or more passes thru the two filters

Only 3 - 10 ppm incident power leaks from one band to the other

Production Sample Measurements over Temperature
Miniaturization Through Microcap Wafer-Level Packaging

- Cap Wafer
- Bonded Wafer
- Individually Sealed Filters
- Microcap’d die ready for assembly in modules

- Wafer to wafer bond
- Wafer-scale batch process
- Assembly can be wire bond or SMT
- Sold as die or integrated into module

For molded chip-on-board (MCOB) package assembly
Chip-Scale Packaged FBAR Oscillator

**Technology Features:**
- High frequency (500MHz to 5GHz), high Q, FBAR resonator with temperature compensation
- Oscillator circuitry (Bipolar, CMOS, SiGe BiCMOS, etc) integrated into lid

**Best in Class Performance:**
- Jitter <10 fsec at GHz frequencies, with current consumption <20 mA
- Differential (or single-ended) output

**Proven Manufacturability:**
- Borrows from standard microcap, FBAR, and IC processes
FBAR Oscillator Chip-Scale Package Design

Can be integrated directly into a customer’s ASIC package

3 x 2 pad array (6 pin package)
Cu/ENIG pads for flip-chip
Form-factor: 1.07 x 0.90 x 0.23 mm
Most oscillator designs require 3 to 4 external SMD’s
Value Proposition of FBAR Chip-Scale Oscillator

- High native frequency (500 MHz to 5 GHz): 10 to 100X higher than Quartz.

- Extremely low jitter (< 10 fsec): 10 to 100X better than Quartz.

- Very small chip-scale hermetic package: 10X smaller than Quartz.

- Exceptional vibration performance (< 1ppb/g): nearly 10X better than Quartz.

- High volume manufacturing, with excellent reliability.
Why Low Phase Noise Oscillators?

- Upcoming communication systems will be more difficult and expensive to design (e.g. 100GE):
  - Board materials, routing, connectors, power supplies
  - Interoperability, standards, margin at high speeds
  - Labor and schedule, expertise

- Temporal link budgets can be relieved by starting with a cleaner reference oscillator:
  - Spend the difference in other areas
  - Reduce cost, and increase reliability
  - Higher modulation complexity demands cleaner oscillators
FBAR Oscillator Phase Noise: Before & After Divide by 4

FBAR oscillator native frequency is 2577.4 MHz. Used an external PECL divide-by-four chip to divide frequency down to 644 MHz.

Single Side Band Phase Noise (dBc/Hz)

- < 10 fsec RJ at 2577 MHz
- ~40 fsec RJ at 644 MHz

Supportable by typical ASIC on-die clock trees.

At native frequency of 2577 MHz, random jitter is <10 fsec.

After dividing by four to 644 MHz, random jitter is ~40 fsec.
FBAR oscillator produces 34X less RJrms.

Dramatically better in mid-range and far-from-carrier.

Close-in performance is less of an issue for modern PLL-based serial communication systems.
Measuring SerDes TX Performance (at 13 GHz)

- Evaluated raw TX performance of a production SerDes ASSP

- Each oscillator programmed to 644 MHz as reference clock for an Avago AVSP-8801 8-channel 1-28 Gbps re-timer

- DIV40 to produce bit rate of 25.78125 Gbps, 0101 pattern (12.89 GHz)

- Using Agilent E4448A spectrum analyzer with phase noise module
Comparison of SerDes TX Driven by Three Reference Oscillators

Freq = 13 GHz

The trend and advantage remain with the FBAR oscillator:
- We demonstrate a 13 GHz clock with only 179 fsec of RJ_{rms}
- On-die effects (power supply and switching noise) add to the jitter
- Approx 2X better jitter even after 40X multiplication
- Future co-design can recover some of FBAR oscillator low jitter
Impact of Reference Oscillator on SerDes TX Jitter Performance

- Key Question: is jitter-performance improvement in reference oscillator lost through PLLs in SerDes and Optical Converters?

Tests comparing FBAR oscillator to commercial oscillators are compelling: jitter improvement ranges from ~15 to 40%.

On-die effects of the target application do not swamp out the benefits of the cleaner source.

Short Answer → Reference Clock Jitter performance matters
HiFi-25GEM test platform:
- 15 channel 1-28 Gbps AVSP-521
- 12 channel pre-alpha 25.78 Gbps embedded optics platform
- Variety of copper channels (Megtron 6)
- Optical ribbon cable (1m) & FO (100m)
- Power / Ethernet-control / misc

Experiments (Goal: CDRs Off for Power Savings)
- Clock from Si5338 vs FBAR oscillator
- PRBS31 at 26 Gbps, aggressors ON
- Various copper and optical channel combinations
- Optical CDRs ON and OFF
FFE, DFE, CTLE, Pre-Amps, and PLL settings are optimized in the SerDes chip prior to each run.
Overview of Full System Test

- Measured eye diagram (CDF) at final receiver in chain, comparing FBAR oscillator to si5338:
  - Receiver stress tolerance including pre-amp, DFE, etc
  - Modern SerDes on-die functions allow these evaluations in a closed-loop system

- Horizontal and vertical bathtub curves:
  - Projected bit error rates, eye closure, RJ, DJ, RVN, DVN
  - Using Dual-Dirac model, in Q-function space, as correct statistical method
  - Even so, this technique has limited accuracy (but avoids multi-day bit error tests, so worth it)
Eye Diagram Measurements
(1e9 samples / pxl)

RX CDR ON, TX CDR OFF

FBAR Oscillator
Q=7 Extrapolation → 165 mUI RJ
Si5338
Q=7 Extrapolation → 82 mUI RJ

All CDRs OFF

FBAR Oscillator
Q=7 Extrapolation → 109 mUI RJ
Si5338
Q=7 Extrapolation → 78 mUI RJ
Horizontal Bathtub Extrapolations
(1e9 samples / pxl, extrapolate to Q = 7 or BER = 1e-12)

RX CDR ON, TX CDR OFF

FBAR Oscillator

165 mUI RJ (at Q = 7)

Si5338

82 mUI RJ (at Q = 7)

With RX CDR on, RJ is 2x better with FBAR oscillator.

All CDRs OFF

FBAR Oscillator

109 mUI RJ (at Q = 7)

Si5338

78 mUI RJ (at Q = 7)

With all CDRs off, RJ is 40% better with FBAR oscillator.
Summary

- We have demonstrated an ultra-small, low-jitter CSP oscillator based on FBAR. Leverages high volume manufacturing.
- We have evaluated the FBAR oscillator in a 26 GHz optical module with one or both CDRs turned off.
- *Compelling* jitter performance advantages were demonstrated – all the way through a complex real-world communication link.

Potential to **Co-Locate** low noise Reference Clock with ASIC:
- Reduces SJ, DCD, and RJ ‘jitter amplification’
- Eliminates possibility of ‘jitter pick-up’ from adjacent data lines

Potential for **Co-Design** with ASIC:
- Power savings, PLL design
- On-chip clock tree design (1.25 GHz, 2.5 GHz oscillator frequency)