Verification Challenges for Backplane Autonegotiation

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AGENDA

- Overview of Ethernet and Auto Negotiation (AN)
- Verification requirements for Auto Negotiation
- Verification strategy for AN layer
ABSTRACT

- UVM based comprehensive metric driven verification (MDV) approach for functional verification of backplane Auto-Negotiation (AN) using coverage and checks (assertions)
OSI model and Ethernet

Sub-Layer
- PCS/PMA

PMD
- Clause 72 Training

Autoneg
- Clause 73 Backplane

Interaction with PMD layer

Auto-Neg is asynchronous

AN is last sub-layer that resolves the underlying PHY interface
Complexity of AN Layer

Where do I start from?

10 FSM states with 21 transitions

Link Failure Verification

“...RESET causes end of simulation and does not result in a restart...”

Simulation hangs if I restart PMD training

Interaction with PMD link Training

How will my design behave if the link goes down in the middle of a simulation?

Re-negotiation at link break up

My chip failed on silicon

DME Page verification

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CL73 AN Verification

DME Page

Capability Exchange

Error injection

Timing and Asynchronous restarts

Link Code word, Ability Exchange, MDIO interface

Custom features/Next Page
Timing and DME Pages

Link codeword → DME page encoding

Advertise Technology Ability Field → Advertise Pause Ability → DME page bit transmission

DME Page Errors:
- Page size error
- Bit corruption error

DME page timing errors:
- Delimiter violation
- Bit cell boundary violation

Forward Error Correction
Physical layer selection based on the Technology ability field

Functional capability using priority resolution

Ensuring link partner sync using nonce and acknowledge match

Next page transmission
ERROR INJECTION

Illegal /Reset Scenario Handling

Static Error Injection
- DME Page Length
- DME Clock Bit Error
- Timers Expiry

Dynamic Error Injection
- Nonce Match
- ACK bit change
- Run time change of LCW

Reset and Restart Handling
- Graceful reset handling
- Restart Handling from all AN states
Verification Environment

- CL73 Tx FSM
- CL73 Arbitration FSM
- CL73 Rx FSM
- Test Scenario Bank
- Configuration
- Coverage Engine
- Assertion Engine
- Pin level Interface
- Testbench Interface
- DUT
Metric Driven Verification

Setup and configuration
- Ease of integration
- Automated Verification Plan
- Automated test suite generation

Test Suite and Vplan
- Constrained random test suite
- Directed testcases
- Self checking test suite
- Parameterized VPlan

- Protocol compliance checks
- 100% functional coverage
- Metric based verification closure
Conclusion

- AN verification is complex.
- Metric Driven Verification approach can help in easy and faster closure of verification.
THANK YOU

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